WHAT IS CLAIMED IS:

1. A semiconductor storage device comprising:

a charge pump device; and

a memory cell array to which an output from an output line of the charge pump device is fed and which uses nonvolatile memory elements as memory cells,

wherein the charge pump device has:

k (where k is a positive integer equal to or more than 2) charge pumps which are connected between an input line and the output line;

output-side switch means for electrically connecting or disconnecting respective output terminals of the k charge pumps to or from the output line;

input-side switch means for electrically connecting or disconnecting input respective terminals of the charge pumps except one charge pump, respectively, to or from the input line; and

series-connection switch means for electrically connecting or disconnecting the output terminal of an nth (where n is an integer of 1 to k-1) charge pump to or from the input terminal of an (n+1)th charge pump, and

wherein the nonvolatile memory elements each have:

a gate electrode formed on a semiconductor layer with a gate insulator disposed therebetween;

a channel region placed under the gate electrode with the gate insulator disposed therebetween;

diffusion regions placed on opposite sides of the channel region, respectively, and having a conductive type opposite to that of the channel region; and

memory-function bodies formed on opposite sides of the gate electrode, respectively, and having a function of holding electric charges.

2. The semiconductor storage device as claimed in Claim 1, wherein

the output-side switch means includes output-side switches provided on lines, respectively, that connect the individual output terminals of the charge pumps to the output line;

the input-side switch means includes input-side switches provided on lines, respectively, that connect the individual input terminals of the charge pumps except the one charge pump to the input line; and

the series-connection switch means includes a series-connection switch provided on a line that connects the output terminal of the nth charge pump to the input terminal of the (n+1)th charge pump.

3. The semiconductor storage device as claimed in Claim 1, wherein

the k charge pumps include first and second charge pumps;

the output-side switch means includes a first output-side switch provided on a line that connects the output terminal of the first charge pump to the output line, and a second output-side switch provided on a line that connects the output terminal of the second charge pump to the output line;

the input-side switch means includes an input-side switch provided on a line that connects the input terminal of the second charge pump to the input line; and

the series-connection switch means includes a series-connection switch provided on a line that connects the output terminal of the first charge pump and the input terminal of the second charge pump.

4. The semiconductor storage device as claimed in Claim 1, wherein the output-side switch means comprises diode-connected field-effect transistors.

5. The semiconductor storage device as claimed in Claim 1, wherein at least one of the k charge pumps includes a plurality of pump stages connected in series.

6. The semiconductor storage device as claimed in Claim 1, further comprising:

at least one voltage polarity inversion circuit provided on a line that connects an output terminal of the

semiconductor storage device and an input terminal of the memory cell array.

7. The semiconductor storage device as claimed in Claim 1, wherein at least part of the memory function bodies owned by the memory element overlaps with part of the diffusion regions.

8. The semiconductor storage device as claimed in Claim 1, wherein the memory function bodies of each nonvolatile memory element each include:

a film having a surface roughly parallel to a surface of the gate insulation film and having a function of retaining electric charges; and

an insulation film separating the film having the function of retaining electric charges from the channel region or the semiconductor layer,

the insulation film having a film thickness thinner than a film thickness of the gate insulation film and not smaller than 0.8 nm.

9. Portable electronic equipment having the semiconductor storage device claimed in claim 1.